In the Specification

Amend the paragraph on page 1, lines 6 to 9 to read as follows:

This application is related to U.S. Patent Application Serial No. 10/696,539 ~~(Attorney Docket No. TI-36031~~, filed on October 23, 2003, ~~~~, entitled TRIPLE GATE MOSFET TRANSISTOR AND METHODS FOR FABRICATING THE SAME.

Amend the paragraph from page 2, line 27 to page 3, line 13 to read as follows:

As the performance and process limitations on scaling planar transistors are reached, attention has been recently directed to transistor designs having multiple gates (*e.g.*, non-planar MOS transistors). In theory, these designs provide more control over a scaled channel by situating the gate around two or more sides of the channel silicon, wherein a shorter channel length can be achieved for the same gate dielectric thickness or similar channel lengths can be used with thicker gate dielectrics. Figs. 11a and 11B ~~10A and 10B~~ illustrate examples of some multiple-gate transistor designs, including dual and triple-gate transistors 60 and 62, respectively in Fig. 11A ~~10A~~, as well as a quad-gate transistor 64, and a "PI"-gate transistor 66 in Fig. 11B ~~10B~~, formed in a silicon over insulator (SOI) wafer 68. In conventional multi-gate devices, an SOI wafer is provided, which includes a substrate with an overlying oxide insulator and a 20.0-50.0 nm thick semiconductor layer above the oxide. The upper silicon layer is etched away, leaving isolated islands or blocks of silicon, and a gate is formed around the silicon blocks, with the ends of the blocks being doped to form source/drains, as illustrated in Figs. 11A and 11B ~~10A and 10B.~~

Amend the paragraph bridging pages 17 and 18 as follows:

In Figs. 6A-6C, the form structure 108 is removed, for example, by wet etching or other process, leaving the semiconductor body 110 disposed above the substrate 104. A gate oxide 112 is formed in Figs. 7A-7C over the semiconductor body 110 and a gate electrode material layer 114 (*e.g.*, polysilicon, metal, or other suitable material) is deposited over the gate dielectric 112. The gate is etched in Figs. 8A-8C to remove portions of the gate electrode material 114 from the first and third body portions 110a and 110c, respectively. The gate etch also ~~to~~ removes the material 114 over part of the second body portion 110b to leave a patterned gate structure having a gate length 114_L corresponding to the channel length 110_L, wherein the gate etch may, but need not, remove portions of the gate dielectric 112. In the illustrated example, the gate length 114_L roughly corresponds to the channel structure depth 110_D (*e.g.*, about 25 nm or less in the exemplary device 100), wherein the semiconductor body 110_W is less than the gate length 114_L.